WHAT IS CLAIMED IS:

1. A stacked IC comprising:

a first IC package unit comprising an IC chip, an encapsulant resin and a plurality of lead wires, said IC chip being encapsulated by said encapsulant resin, wherein each of said lead wires comprises a first end connected to said IC chip and encapsulated by said encapsulant resin and a second end extending outside said encapsulant resin, wherein said second end extending outside said encapsulant resin comprises first and second soldering portions;

a second IC package unit having the same structure as said first IC package unit; and

an interface layer sandwiched between said first IC package unit and said second IC package unit, and having first and second sides with a plurality of soldering pads, wherein each first soldering portion of said first IC package unit is connected to corresponding soldering pad on said first side of said interface layer via a solder ball, and each second soldering portion of said second IC package unit is connected to corresponding soldering pad on said second side of said interface layer via a soldering material other than said solder ball, thereby achieving electrical connection between said first IC package unit and said second IC package unit.

2. The stacked IC according to claim 1 wherein said first and said second soldering portions are in the vicinity of and distant from said encapsulant resin, respectively.

3. The stacked IC according to claim 1 wherein each of said first and said second soldering portions is substantially parallel to said interface layer.

4. The stacked IC according to claim 1 wherein said interface layer is made of a hard dielectric material.

5. The stacked IC according to claim 1 wherein said interface layer is made of a soft dielectric material.

6. The stacked IC according to claim 1 wherein said IC chip for each of said first IC package unit and said second IC package unit is selected from a group consisting of a memory chip, an application specific integrated circuit (ASIC) chip and a driving integrated circuit chip.

7. The stacked IC according to claim 1 wherein each of said first IC package unit and said second IC package unit is a thin small outline package (TSOP).

8. The stacked IC according to claim 1 wherein each of said first IC package unit and said second IC package unit is a quad flat pack (QFP).

9. A stacked IC comprising:

a first IC package unit comprising an IC chip, an encapsulant resin and a plurality of lead wires, said IC chip being encapsulated by said encapsulant resin, wherein each of said lead wires comprises a first end connected to said IC chip and encapsulated by said encapsulant resin and a second end extending outside said encapsulant resin;

a second IC package unit; and

an interface layer having a first side connected to soldering portions of said lead wires of said first IC package unit via a plurality of solder balls and a second side connected to said second IC package unit.

10. The stacked IC according to claim 9 wherein said interface layer is made of a hard dielectric material.

11. The stacked IC according to claim 9 wherein said interface layer is made of a soft dielectric material.

12. The stacked IC according to claim 9 wherein said IC chip is selected from a group consisting of a memory chip, an application specific integrated circuit

(ASIC) chip and a driving integrated circuit chip.

13. The stacked IC according to claim 9 wherein said first IC package unit is selected from a group consisting of a thin small outline package (TSOP), a quad flat pack (QFP), a small outline package (SOP), a pin grid array (PGA), and a small outline package J-leaded package (SOJ).

14. The stacked IC according to claim 9 wherein said second IC package unit is selected from a group consisting of a thin small outline package (TSOP), a quad flat pack (QFP), a ball grid array (BGA), a small outline package (SOP), a pin grid array (PGA), and small outline package J-leaded package (SOJ).

15. A stacked IC comprising:

a first IC package unit selected from a group consisting of a thin small outline package (TSOP), a quad flat pack (QFP), a small outline package (SOP), a pin grid array (PGA), and a small outline package J-leaded package (SOJ);

a second IC package unit selected from a group consisting of a thin small outline package (TSOP), a quad flat pack (QFP), a ball grid array (BGA), a small outline package (SOP), a pin grid array (PGA), and a small outline package J-leaded package (SOJ); and

an interface layer having a first side connected to said first IC package unit via a plurality of solder balls and a second side connected to said second IC package unit.

16. The stacked IC according to claim 15 wherein said interface layer is made of a hard dielectric material.

17. The stacked IC according to claim 15 wherein said interface layer is made of a soft dielectric material.

18. The stacked IC according to claim 15 wherein said IC chip is selected from a group consisting of a memory chip, an application specific integrated circuit

(ASIC) chip and a driving integrated circuit chip.